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MC68HC908EY16

The MC68HC908EY16 microcontroller is the first in a family of high performance 8-bit microcontrollers targeted at LIN based solutions and general market applications.

Offering 16K bytes of high performance Flash memory, future family derivatives will provide full pin compatibility and a range of Flash based program memories.

This document provides an overview of the features of the MC68HC908EY16. Further details are available in the advance information data book which is available on request.

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1 Introduction

The MC68HC908EY16 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

2 Features

For convenience, features have been organized to reflect:

- Standard features of the MC68HC908EY16

- Features of the CPU08

Standard features of the MC68HC908EY16 include:

- High-performance M68HC08 architecture optimized for C-compilers

- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families

- 8-MHz internal bus frequency at 5V, 4MHZ at 3V

- Internal oscillator requiring no external components:

    – Software selectable bus frequencies

    – 25 percent accuracy with trim capability to 2 percent

    – Clock monitor

    – Option to allow use of external clock source or external crystal/ceramic resonator

- 15,872 bytes of on-chip FLASH memory with in-circuit programming

- FLASH program memory security[1]

- 512 bytes of on-chip random-access memory (RAM)

- Low voltage inhibit (LVI) module with software selectable trip points for 5V and 3V operation.

- Internal clock generator module (ICG)

- Two 16-bit, 2-channel timer (TIMA and TIMB) interface modules with selectable input capture, output compare, and pulse-width modulation (PWM) capability on each channel

- 8-channel, 10-bit successive approximation analog-to-digital converter (ADC)

- Enhanced serial communications interface module (ESCI) for local interconnect network (LIN) connectivity

- Serial peripheral interface (SPI)

- Timebase Module (TBM)

- 5-bit keyboard interrupt (KBI) with wakeup feature

- 24 general-purpose input/output (I/O) pins

- External asynchronous interrupt pin with internal pullup (IRQB)

- System protection features:

  – Optional computer operating properly (COP) reset

  – Illegal opcode detection with reset

  – Illegal address detection with reset

- 32-pin quad flat pack (QFP) package

- Low-power design; fully static with stop and wait modes

- Internal pullups on IRQB and RSTB to reduce customer system cost

- Standard low-power modes of operation:

  – Wait mode

  – Stop mode

- Master reset pin (RSTB) and power-on reset (POR)

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1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- BREAK module (BRK) to allow single breakpoint setting during in-circuit debugging

- Higher current source capability on nine port lines for LED drive (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KDB4}$, PTA3/$\overline{KBD3}$, PTA2/$\overline{KBD2}$, PTA1/$\overline{KBD1}$, PTA0/$\overline{KBD0}$, PTC1/MOSI, and PTC0/MISO)

Features of the CPU08 include:

- Enhanced HC05 programming model

- Extensive loop control functions

- 16 addressing modes (eight more than the HC05)

- 16-bit index register and stack pointer

- Memory-to-memory data transfers

- Fast 8×8 multiply instruction

- Fast $16 \div 8$ divide instruction

- Binary-coded decimal (BCD) instructions

- Optimization for controller applications

- Third party C language support

3 MCU Block Diagram
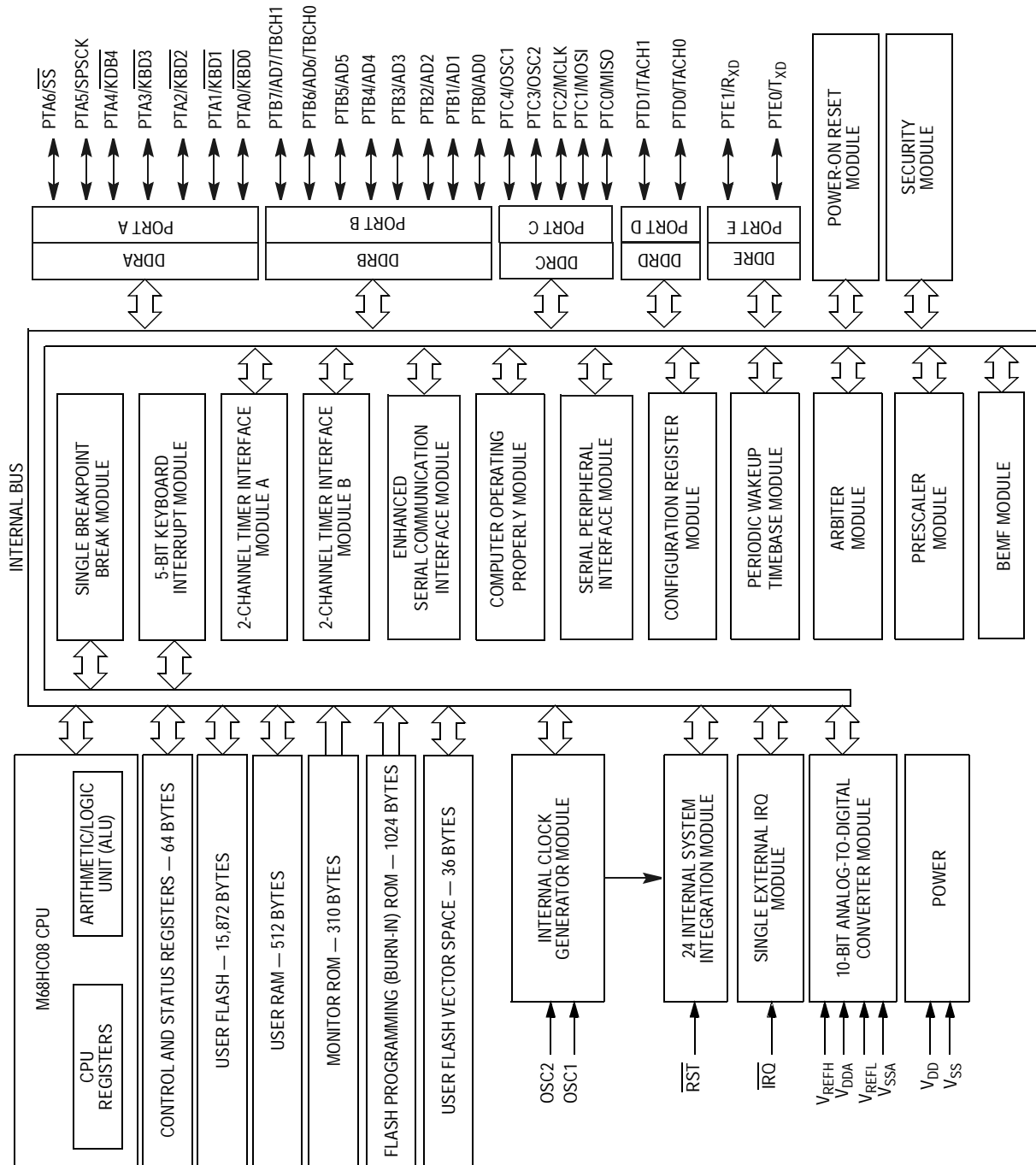
Figure 1 shows the structure of the MC68HC908EY16.

Figure 1. MCU Block Diagram

PTA6/$\overline{SS}$
PTA5/SPSCK
PTA4/$\overline{KBD4}$
PTA3/KBD3
PTA2/KBD2
PTA1/$\overline{KBD1}$
PTA0/$\overline{KBD0}$
PTB7/AD7/TBCH1
PTB6/AD6/TBCH0
PTB5/AD5
PTB4/AD4
PTB3/AD3
PTB2/AD2
PTB1/AD1
PTB0/AD0
PTC4/OSC1
PTC3/OSC2
PTC2/MCLK
PTC1/MOSI
PTC0/MISO
PTD1/TACH1
PTD0/TACH0
PTE1/R$_{XD}$
PTE0/T$_{XD}$

DDRA — PORT A
DDRB — PORT B
DDRC — PORT C
DDRD — PORT D
DDRE — PORT E
POWER-ON RESET MODULE
SECURITY MODULE

INTERNAL BUS

SINGLE BREAKPOINT BREAK MODULE
5-BIT KEYBOARD INTERRUPT MODULE
2-CHANNEL TIMER INTERFACE MODULE A
2-CHANNEL TIMER INTERFACE MODULE B
ENHANCED SERIAL COMMUNICATION INTERFACE MODULE
COMPUTER OPERATING PROPERLY MODULE
SERIAL PERIPHERAL INTERFACE MODULE
CONFIGURATION REGISTER MODULE
PERIODIC WAKEUP TIMEBASE MODULE
ARBITER MODULE
PRESCALER MODULE
BEMF MODULE

M68HC08 CPU
CPU REGISTERS
ARITHMETIC/LOGIC UNIT (ALU)
CONTROL AND STATUS REGISTERS — 64 BYTES
USER FLASH — 15,872 BYTES
USER RAM — 512 BYTES
MONITOR ROM — 310 BYTES
FLASH PROGRAMMING (BURN-IN) ROM — 1024 BYTES
USER FLASH VECTOR SPACE — 36 BYTES

INTERNAL CLOCK GENERATOR MODULE
24 INTERNAL SYSTEM INTEGRATION MODULE
SINGLE EXTERNAL IRQ MODULE
10-BIT ANALOG-TO-DIGITAL CONVERTER MODULE
POWER

OSC2
OSC1
$\overline{RST}$
$\overline{IRQ}$
V$_{REFH}$
V$_{DDA}$
V$_{REFL}$
V$_{SSA}$
V$_{DD}$
V$_{SS}$

Product Summary

4 Pin Assignments

Figure 2 shows the pin assignments for the MC68HC908EY16.
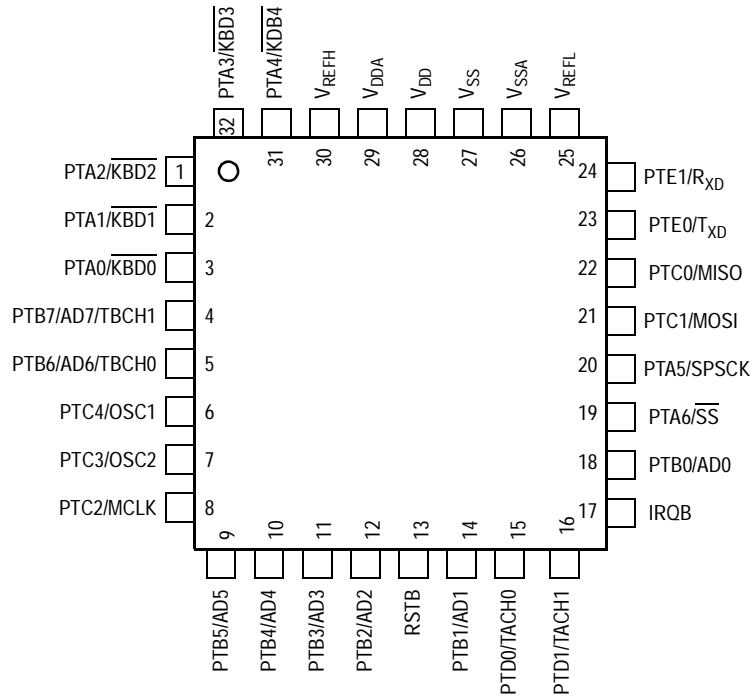

Figure 2. Pin Assignments

5 Pin Functions

Descriptions of the pin functions are provided here.

5.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as **Figure 3** shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.
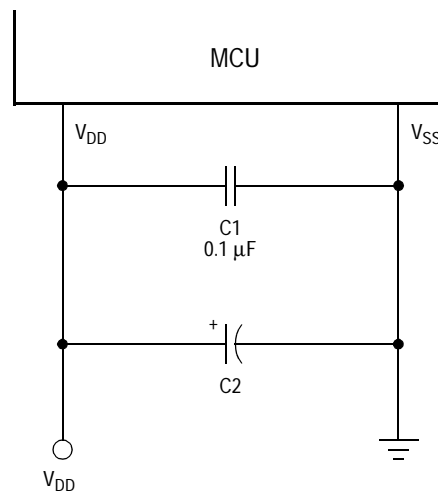
Note: Component values shown represent typical applications.

Figure 3. Power Supply Bypassing

5.2 Oscillator Pins (PTC4/OSC1 and PTC3/OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator.

When selecting PTC4 and PTC3 as I/O, OSC1 and OSC2 functions are not available.

5.3 External Reset Pin (RSTB)

A logic 0 on the RSTB pin forces the MCU to a known startup state. RSTB is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This pin contains an internal pullup resistor that is always activated, even when the reset pin is pulled low.

5.4 External Interrupt Pin (IRQB)

IRQB is an asynchronous external interrupt pin. This pin contains an internal pullup resistor that is always activated, even when the IRQB pin is pulled low.

5.5 Analog Power Supply/Reference Pins (V_{DDA}, V_{REFH}, V_{SSA} and V_{REFL})

V_{DDA} and V_{SSA} are the power supply pins for the analog-to-digital converter (ADC). Decoupling of these pins should be as per the digital supply.

NOTE: V_{REFH} is the high reference supply for the ADC. V_{DDA} should be tied to the same potential as V_{DD} via separate traces.

V_{REFL} is the low reference supply for the ADC. V_{SSA} should be tied to the same potential as V_{SS} via separate traces.

5.6 Port A I/O Pins (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KDB4}$–PTA0/$\overline{KBD0}$)

Port A input/output (I/O) pins (PTA6/$\overline{SS}$, PTA5/SPSCK, PTA4/$\overline{KDB4}$, PTA3/$\overline{KBD3}$, PTA2/$\overline{KBD2}$, PTA1/$\overline{KBD1}$, and PTA0/$\overline{KBD0}$) are special-function, bidirectional I/O port pins. PTA5 and PTA6 are shared with the serial peripheral interface (SPI). PTA4-PTA0 can be programmed to serve as keyboard interrupt pins.

5.7 Port B I/O Pins (PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, PTB5/AD5–PTB0/AD0)

PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, and PTB5/AD5–PTB0/AD0 are special-function, bidirectional I/O port pins that can also be used for ADC inputs. PTB7/AD7/TBCH1 and PTB6/AD6/TBCH0 are special function bidirectional I/O port pins that can also be used for timer interface pins.

5.8 Port C I/O Pins (PTC4/OSC1, PTC3/OSC2, PTC2/MCLK, PTC1/MOSI, PTC0/MISO)

PTC4/OSC1–PTC0/MISO are special-function, bidirectional I/O port pins. PTC3/OSC2 and PTC4/OSC1 are shared with the on-chip oscillator circuit through configuration options.

When applications require:

- PTC3/OSC2 can be programmed to be OSC2
- PTC4/OSC1 can be programmed to be OSC1

PTC2/MCLK is software selectable to be MCLK, or bus clock out. PTC1/MOSI can be programmed to be the MOSI signal for the SPI. PTC0/MISO can be programmed to be the MISO signal for the SPI.

5.9 Port D I/O Pins (PTD1/TACH1–PTD0/TACH0)

PTD1/TACH1–PTD0/TACH0 are special-function, bidirectional I/O port pins that can also be programmed to be timer pins.

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5.10 Port E I/O Pins (PTE1/R$_{XD}$–PTE0/T$_{XD}$)

PTE1/R$_{XD}$–PTE0/T$_{XD}$ are special-function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication interface (ESCI) pins.

NOTE: *Any unused inputs and I/O ports should be tied to an appropriate logic level (either V$_{DD}$ or V$_{SS}$). Although the I/O ports of the MC68HC908EY16 do not require termination, termination is recommended to reduce the possibility of electro-static discharge damage.*

6 Revision History

The following table gives a summary of revision changes through the history of this document.

Table 1. Summary of Changes

Revision	Section	Description of Change
1.0	2.0	LVI, ICG and TBM added to features list
1.0	2.0	PTA6/$\overline{SS}$ added to list of pins with high current source capability in features list
1.0	3.0	Block diagram revised
1.0	4.0	Pinout revised
1.0	5.5	Analog power supply pin descriptions revised
1.0	5.6–5.10	Minor changes to wording of port pin descriptions for clarification

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